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EXAMINER	
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ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/561,454	ALBA PINTO ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-11 are pending.

2. The office acknowledges the following papers:

Patent Application filed on 12/20/2005.

3. The references cited in the Search Report issued on 8/14/2007 by the EPO have been considered, but will not be listed on any patent resulting from this application because they were not provided on a separate list in compliance with 37 CFR 1.98(a)(1). In order to have the references printed on such resulting patent, a separate listing, preferably on a PTO/SB/08A and 08B form, must be filed within the set period for reply to this Office action.

4. The listing of references in the Search Report is not considered to be an information disclosure statement (IDS) complying with 37 CFR 1.98. 37 CFR 1.98(a)(2) requires a legible copy of: (1) each foreign patent; (2) each publication or that portion which caused it to be listed; (3) for each cited pending U.S. application, the application specification including claims, and any drawing of the application, or that portion of the application which caused it to be listed including any claims directed to that portion, unless the cited pending U.S. application is stored in the Image File Wrapper (IFW) system; and (4) all other information, or that portion which caused it to be listed. In addition, each IDS must include a list of all patents, publications, applications, or other information submitted for consideration by the Office (see 37 CFR 1.98(a)(1) and (b)), and MPEP § 609.04(a), subsection I. states, "the list ... must be submitted on a separate paper." Therefore, the non-patent literature cited in the Search Report has not

been considered. Applicant is advised that the date of submission of any item of information or any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the IDS, including all "statement" requirements of 37 CFR 1.97(e). See MPEP § 609.05(a).

Priority

5. The effective filing date for the subject matter defined in the pending claims in this application is 6/25/2003.

Drawings

6. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitations from claims 1-11 must be shown or the feature(s) canceled from the claim(s). The drawing objections for all of the claimed limitations will be withdrawn when the limitations are labeled within the drawings. No new matter should be entered. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d).

Specification

7. The disclosure is objected to because of the following informalities:

8. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The Applicant's cooperation is requested in correcting any errors of which the Applicant may become aware.

9. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: "Variable clock speed to execute instructions."

10. Appropriate correction is required.

Claim Objections

11. Claim 1-11 are objected to because of the following informalities:

12. Claims 1-11 recite reference to the drawings via figure numbers throughout the claims. All such references should be deleted.

13. Claim 1 line 5 states "an read port" that should be changed to "a read port."

Claim Rejections - 35 USC § 112

14. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

15. Claim 1-8 and 10-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

16. Claim 1 recites the limitation "the other functional units" in lines 9-10 of the claim. There is insufficient antecedent basis for this limitation in the claim.

17. Claim 4 recites the limitation "the latency" in line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim.

18. Claim 10 recites the limitation "the processing task" in line 10 of the claim. There is insufficient antecedent basis for this limitation in the claim.

19. Claim 10 recites the limitation "the task" in line 11 of the claim. There is insufficient antecedent basis for this limitation in the claim.

20. Claim 10 recites the limitation "the first type" in line 12 of the claim. There is insufficient antecedent basis for this limitation in the claim.

21. Claim 11 recites the limitation "the further functional units" in line 5 of the claim. There is insufficient antecedent basis for this limitation in the claim.

22. Claim 11 recites the limitation "the particular one of the further functional units" in lines 6-7 of the claim. There is insufficient antecedent basis for this limitation in the claim.

23. Claims 2-3 and 5-8 are rejected due to their dependency.

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claims 9 and 11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Rozenshein et al. (U.S. 6,418,527).

26. As per claim 9:

Rozenshein disclosed a method of executing a processing task, the method comprising:

providing a group of functional units (Rozenshein: Figure 3 elements 32 and 34, column 5 lines 9-17),

issuing successive instructions to the group (Rozenshein: Figure 11 element 224, column 6 lines 36-52)(The instruction dispatch unit issues instructions from the instruction set to execution units. It's obvious to one of ordinary skill in the art that instructions are issued each clock cycle.);

executing those of the instructions that are of a first type each with an individual one of the functional units (Rozenshein: Figure 3 element 34, column 5 lines 9-17)(The ALU type instructions are executed by the bit field unit.),

executing an instructions that is of a second type with a first and a second one of the functional units in series (Rozenshein: Figure 6 elements 110 and 112, column 5 lines 30-37)(The MAC instructions are executed in series by a multiplier and an accumulator.);

routing a result of the first one of the functional units to an operand of the second one of the functional units in response to the instruction of the second type (Rozenshein: Figure 6 element 116, column 5 lines 30-37)(The multiplier result data is routed to the accumulator.).

27. As per claim 11:

Rozenshein disclosed a method according to claim 9, comprising:

issuing the successive instructions each as part of a VLIW instruction word that contains a plurality of instructions for respective further functional units (Rozenshein: Figure 13, column 7 lines 18-31)(A VLIW is a long instruction that contains a plurality of instructions within the instruction word. The instruction in figure 13 is an instruction word containing a plurality of instructions. Thus, reading upon a VLIW. It's obvious to one of ordinary skill in the art that the instruction in figure 13 can contain an ALU instruction and a MAC instruction that executes on the functional units of figure 3.);

including in the instruction word that contains the instruction of the second type an further instruction for a particular one of the further functional units (Rozenshein: Figure 13, column 7 lines 18-31)(It's obvious to one of ordinary skill in the art that the instruction in figure 13 can contain an ALU instruction and a MAC instruction that executes on the functional units of figure 3.);

routing a further result of the further instruction from the particular one of the further functional units to a further operand input of the second one of the functional units in response to the instruction of the second type (Rozenshein: Figure 6 element 116, column 5 lines 30-37)(The multiplier result data is routed to the accumulator.).

28. Claims 1-2 and 5-8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Rozenshein et al. (U.S. 6,418,527), in view of Hennessy et al. ("Computer organization and design: the hardware/software interface").

29. As per claim 1:

Rozenshein and Hennessy disclosed an instruction controlled data processing device, the device comprising:

an instruction issue unit, having an issue slot for issuing instructions from an instruction set, the instruction issue unit issuing respective ones of the instructions in successive instruction cycles (Rozenshein: Figure 11 element 224, column 6 lines 36-52)(The instruction dispatch unit issues instructions from the instruction set to execution units. It's obvious to one of ordinary skill in the art that instructions are issued each clock cycle.);

a register file with an read port and a write port (Rozenshein: Figure 3 elements 28-29 and 62-64, column 5 lines 9-17)(The register file has read and write ports.);

a group of functional units (Rozenshein: Figure 3 elements 32 and 34, column 5 lines 9-17), each functional unit having a control input coupled to the issue slot (Rozenshein: Figure 3 elements 32 and 34, column 5 lines 9-17)(Hennessy: Figure 6.30, page 469)(The combination results in the control signals shown in Hennessy being used to control the functional units of Rozenshein.), an operand input coupled to the read port and a result output coupled to the write port (Rozenshein: Figure 3 elements 32 and 34, column 5 lines 9-17)(The inputs and outputs are coupled to the register files ports.), each functional unit being arranged to respond to instructions from a respective sub-set of the instruction set to which the other functional units do not respond (Rozenshein: Figure 3 elements 32 and 34, column 5 lines 9-17)(The MAC unit performs MAC operations and the bit field unit performs other ALU operations.), the instruction set further comprising a combination instruction to which a first and second

one of the functional units respond (Rozenshein: Figure 6 elements 110 and 112, column 5 lines 30-37)(The MAC unit performs multiplication and addition.);

a control unit coupled to the issue slot and responsive to the combination instruction from the instruction set, to route the result output of the first one of the functional units to the operand input of the second one of the functional units (Rozenshein: Figure 6 element 116, column 30 lines 30-37)(Hennessy: Figure 6.28 and 6.29, page 469)(The combination uses the control signals of Hennessy to perform control operations in the processor of Rozenshein. This allows for the data bypass of the multiplier to the adder.).

The processor of Rozenshein failed to show the inherent control signals that are present to control the processor operations according to the decoded instructions. One of ordinary skill in the art would have been motivated by this lack of teaching by Rozenshein to find Hennessy that discloses how a control unit controls the operations of a processor. Thus, one of ordinary skill in the art at the time of the invention would have been motivated to add the control signals of Hennessy to the processor of Rozenshein to show how all of the processor logic units are controlled during operation.

30. As per claim 2:

Rozenshein and Hennessy disclosed an instruction controlled data processing device according to claim 1, organized as a VLIW processor, the issue slot being one of a plurality of issue slots of the instruction issue unit for issuing a VLIW instruction word that contains the combination instruction as one of its instructions (Rozenshein: Figure 13, column 7 lines 18-31)(A VLIW is a long instruction that contains a plurality of

instructions within the instruction word. The instruction in figure 13 is an instruction word containing a plurality of instructions. Thus, reading upon a VLIW. It's obvious to one of ordinary skill in the art that the instruction in figure 13 can contain an ALU instruction and a MAC instruction that executes on the functional units of figure 3.), the register file having a plurality of sets of read and write ports, the device comprising respective functional units or groups of functional units each coupled to a respective one of the issue slots and the sets of read and write ports for executing respective instructions from the VLIW instruction word (Rozenshein: Figure 3 elements 28-29 and 62-64, column 5 lines 9-17)(The register file has read and write ports.), the first and second one of the functional units in responding to the combination instruction issued in the issue slot in parallel with execution of instructions issued in the same instruction word as the combination instruction (Rozenshein: Figures 3 and 13 elements 32 and 34, column 7 lines 18-31)(The instructions in the long instruction word of figure 13 are executed in parallel.).

31. As per claim 5:

Rozenshein and Hennessy disclosed an instruction controlled data processing device according to claim 1, wherein the instruction issue unit has a further issue slot and the register file has a further read port, the device comprising a further functional unit having a control input coupled to the further issue slot and an operand input coupled to the further read port, the control unit being arranged to route the result output of the further functional units to a further operand input of the second one of the functional units under control of the combination instruction, bypassing the register file

under control of the combination instruction (Rozenshein: Figure 6 elements 110 and 112, column 5 lines 30-37)(Hennessy: Figure 6.28 and 6.29, page 469)(The combination uses the control signals of Hennessy to perform control operations in the processor of Rozenshein. This allows for the data bypass of the multiplier to the adder.).

32. As per claim 6:

Rozenshein and Hennessy disclosed an instruction controlled data processing device according to claim 5, programmed with a program that contains a VLIW instruction that contains a command for the further functional unit and the combination instruction for the group of functional units for issue in a same instruction cycle (Rozenshein: Figure 13, column 7 lines 18-31)(A VLIW is a long instruction that contains a plurality of instructions within the instruction word. The instruction in figure 13 is an instruction word containing a plurality of instructions. Thus, reading upon a VLIW. It's obvious to one of ordinary skill in the art that the instruction in figure 13 can contain an ALU instruction and a MAC instruction that executes on the functional units of figure 3.).

33. As per claim 7:

Rozenshein and Hennessy disclosed an instruction controlled data processing device according to claim 1, wherein the control unit is arranged to make the second one of the functional units respond to the combination instruction in an instruction execution cycle following an instruction execution cycle in which the first one of the functional units responds to the combination instruction (Rozenshein: Figure 6 elements

110 and 112, column 5 lines 30-37)(Hennessy: Figure 6.28 and 6.29, page 469)(The MAC operations occurs by performing the multiply and accumulate operations in sequential order. The combination uses the control unit of Hennessy to control the pipelining operations of Rozenshein.).

34. As per claim 8:

Rozenshein and Hennessy disclosed an instruction controlled data processing device according to claim 7, wherein the result of the first one of the functional units is routed without intermediate latching from the first one of the functional units to the operand input of the second one of the functional units (Rozenshein: Figure 6 element 116, column 5 lines 30-37)(The output of the multiplier is bypassed to the accumulator without needing a latch.).

35. Claim 10 is rejected under 35 U.S.C. §103(a) as being unpatentable over Rozenshein et al. (U.S. 6,418,527), further in view of Sager et al. (U.S. 6,487,675).

36. As per claim 10:

Rozenshein disclosed a method according to claim 9, wherein the first and the second one of the functional units respond to the instruction of the second type in a same instruction execution cycle.

Rozenshein failed to teach selecting an instruction cycle rate from at least a first and second rate, the first rate being so slow that execution of a combination instruction by a cascade of at least two of the functional units fits within an instruction cycle at the first rate, the second rate being so fast that only execution of instructions by single ones

of the functional units fits within the instruction execution cycle at the second rate, execution of the combination instruction not fitting within one instruction execution cycle at the second rate and adapting the instructions used to execute the processing task to the selected instruction cycle rate, so that the combination instruction is used when the task is executed at the first rate and the combination instruction is replaced by instructions of the first type with corresponding effect when the task is executed at the second rate.

However, Sager disclosed selecting an instruction cycle rate from at least a first and second rate, the first rate being so slow that execution of a combination instruction by a cascade of at least two of the functional units fits within an instruction cycle at the first rate, the second rate being so fast that only execution of instructions by single ones of the functional units fits within the instruction execution cycle at the second rate, execution of the combination instruction not fitting within one instruction execution cycle at the second rate (Sager: Figure 3 elements 220 and 225, column 4 lines 48-67 continued to column 5 lines 1-6)(The combination results in the bit field operations having a faster clock according to the intolerant sub-core and the MAC unit having a clock according to the tolerant sub-core. This results in the MAC having a longer clock speed than the bit field instructions and results in the MAC operation not being able to be executed by the clock speed of the intolerant sub-core.);

adapting the instructions used to execute the processing task to the selected instruction cycle rate, so that the combination instruction is used when the task is executed at the first rate and the combination instruction is replaced by instructions of

the first type with corresponding effect when the task is executed at the second rate (Rozenshein: Figure 3 elements 32 and 34)(Sager: Figure 3 elements 220 and 225, column 4 lines 48-67 continued to column 5 lines 1-6)(At the slower speed clock, the MAC instruction is performed by the MAC unit in a clock cycle. At the higher speed clock, the MAC instruction can be performed by two separate instructions.)

The advantage of dividing up the processor functions into a plurality of clock speeds allows for the slower speed functions to have a simplified design, which can lead to decreased chip space usage and power savings (Sager: Column 4 lines 3-20). One of ordinary skill in the art would have been motivated by this advantage to implement multiple clock speeds into the processor of Rozenshein. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to implement multiple clock speeds in the processor of Rozenshein for the advantage of decreased chip space usage and power savings.

37. Claim 3 is rejected under 35 U.S.C. §103(a) as being unpatentable over Rozenshein et al. (U.S. 6,418,527), in view of Hennessy et al. ("Computer organization and design: the hardware/software interface"), further in view of Davis (U.S. 6,367,003).

38. As per claim 3:

Rozenshein and Hennessy disclosed an instruction controlled data processing device according to claim 1.

Rozenshein and Hennessy failed to teach wherein the first and second one of the functional units respond to the combination instruction in a same instruction execution cycle.

However, Davis disclosed wherein the first and second one of the functional units respond to the combination instruction in a same instruction execution cycle (Davis: Figure 2, column 1 lines 26-37)(The combination results in using the MAC unit of Davis in the processor of Rozenshein.).

The advantage of the MAC unit of Davis is that it's a faster MAC unit capable of executing an instruction in a single cycle. The advantage of executing MAC instructions faster is that it will result in increased performance overall for a given program. One of ordinary skill in the art would have been motivated by this advantage to implement the fast MAC into Rozenshein. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the fast MAC unit of Davis into the processor of Rozenshein for the advantage of increased performance through executing the MAC instruction in a quicker fashion.

39. Claim 4 is rejected under 35 U.S.C. §103(a) as being unpatentable over Rozenshein et al. (U.S. 6,418,527), in view of Hennessy et al. ("Computer organization and design: the hardware/software interface"), in view of Davis (U.S. 6,367,003), further in view of Sager et al. (U.S. 6,487,675).

40. As per claim 4:

Rozenshein, Hennessy, and Davis disclosed an instruction controlled data processing device according to claim 3.

Rozenshein, Hennessy, and Davis failed to teach comprising a clock circuit for clocking the instruction cycles, the clock circuit having a plurality of selectable clock rates, including a first clock rate that is sufficiently slow to accommodate within an instruction execution cycle the latency involved in producing a result from the second one of the functional units in response to an operand applied to the first one of the functional units also during execution of the combination instruction within the instruction execution cycle, and a second clock rate that is too fast to accommodate said latency in the instruction cycle, but accommodates latency of instructions from said sub-sets.

However, Sager disclosed comprising a clock circuit for clocking the instruction cycles, the clock circuit having a plurality of selectable clock rates, including a first clock rate that is sufficiently slow to accommodate within an instruction execution cycle the latency involved in producing a result from the second one of the functional units in response to an operand applied to the first one of the functional units also during execution of the combination instruction within the instruction execution cycle, and a second clock rate that is too fast to accommodate said latency in the instruction cycle, but accommodates latency of instructions from said sub-sets (Sager: Figure 3 elements 220 and 225, column 4 lines 48-67 continued to column 5 lines 1-6)(The combination results in the bit field operations having a faster clock according to the intolerant sub-core and the MAC unit having a clock according to the tolerant sub-core. This results in

the MAC having a longer clock speed than the bit field instructions and results in the MAC operation not being able to be executed by the clock speed of the intolerant sub-core.).

The advantage of dividing up the processor functions into a plurality of clock speeds allows for the slower speed functions to have a simplified design, which can lead to decreased chip space usage and power savings (Sager: Column 4 lines 3-20). One of ordinary skill in the art would have been motivated by this advantage to implement multiple clock speeds into the processor of Rozenshein. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to implement multiple clock speeds in the processor of Rozenshein for the advantage of decreased chip space usage and power savings.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kuemerle (U.S. 6,457,131), taught adjusting power dependent on decoded instructions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183

/David J. Huisman/
Primary Examiner, Art Unit 2183